Efficient model-based analog circuits sizing

Thierry Lachaud
CAD support Manager – ST Microelectronics
Wireless and multimedia division – 12 rue Jules Horowitz – 38000 Grenoble FRANCE

Vincent Fischer PhD
Product manager-Infiniscale – 55, rue Blaise Pascal 38330 Montbonnot - FRANCE

ABSTRACT
This paper aims at presenting a new model-based flow targeting analog/RF circuits sizing with significant improvements of parametric yield at a very early stage in the design phase. The flow is then applied on a ST Microelectronics [2] LDO regulator design. In a first step, the regulator is modeled. In the second one, the design is optimally sized. The process parameters are then modeled, and finally the sensitivity of the design to the process is analyzed.

1. INTRODUCTION
From a given technological node to the next, parameter dispersion (due to process variations) and optical distortions (from layout to lithography) are strongly increasing.
These phenomena, together with the ever increasing circuit complexity, are impacting on yield and reliability. How to improve them for a nanometer scale process? How to perform efficient predictions and monitoring?
This is actually a major concern of many EDA companies.

Most of these try to tackle these new issues by optimizing OPC at layout level. However, little attention has been paid to parametric yield.
Analyzing process variations, optimizing design parameters and verifying environment conditions at early design stage become mandatory.
In order to address analog circuits sizing and parametric yield, the vast majority of existing tools is simulator-based [9], which make them less efficient for large designs. Accurate sensitivity analysis and yield optimization needs thousands of Monte Carlo runs, which virtually eliminates the possibility of using simulators. Such techniques are still used for local sizing of small cells [3].
Just like process variation verification, traditional pre-defined corners need a large number of simulations and suffer from possible over-design. Statistical Monte-Carlo analysis offers good accuracy, eliminates over-design, but requires a very large number of runs. Thus, the best compromise seems to be performance models extraction based on limited number of simulations and model-based Monte-Carlo analysis and optimization.
InfiniScale [1] Lysis™ environment offers such a flow by relying on a unique and very efficient technology. Based on innovative and cost-effective behavioral modeling techniques, InfiniScale’s flow offers a practical solution for modeling complex non-linear phenomena, feeding a model-based flexible sizing tool, a model-based analysis and yield optimization tool.
Using InfiniScale modeling engine, model-based sizing and optimization solutions at an early stage in the design can improve product performance, yield and reliability at lower cost and in a shorter time than building and testing physical prototypes. Design for Reliability is forming a natural
complement to Design for Yield and offers the opportunity to follow the same approach (statistical in nature).

This article presents the application of the InfiniScale flow as described above onto a LDO (Low Drop Output) regulator cell designed using 65 nanometer technology from STMicroelectronics. The validation study first aims at modeling transient and AC performances with regard to design, environment and process parameters.

2. STATE OF THE ART

The large majority of available analog CAD software are analysis tools. Modeling and sizing remain the bottleneck of analog designs in general and in RF designs in particular.

The majority of classical modeling solutions are based on polynomial models and DoE techniques [4][5][6]. These methods are iterative, and appear to be not efficient and accurate enough to fulfill the challenge towards electronic nanometer scales which implies high number of variables with strong complex interactions or highly non linear behaviors. They are expensive because the number of needed sample points explodes when the number of involved parameters and/or the nonlinearity degree of the phenomenon increase.

Some trials to improve these techniques by introducing posynomial modeling have been made [7][8]. The use of posynoms seem to enhance nonlinear fitting capabilities, but they are still too simulation-consuming.

In [10][11], the authors introduce a projection-based posynomial modeling that allows reducing the number of needed samples for modeling but at the expense of accuracy. It should be noted that this modeling is local and cannot be used for global yield optimization.

Most of yield-oriented EDA existing tools are simulator-based. However, it should be noted that they are limited to small analog cells.

Most design and process analysis tools are based on corners simulation. There is a number of issues with corner analysis. Perhaps the most troublesome one is when the designer is forced to make a best guess. Guessing worst case corners could result in a waste of design time, a larger area, higher power consumption, or even no design at all. Another important problem that appears today with nanometer scales is that corners, even when they are well known, may not cover the entire ranges of a design.

3. THE INFINISCALE FLOW

InfiniScale’s modeling and optimization environment, Lysis™, efficiently tackles these new issues of analog systems design by offering:

- An efficient automatic modeling tool that allows a cost-effective parameterization of your design and technology
- An accurate, fast, model-based and standalone sizer that no more needs large number of expensive simulations.
- A rapid model-based sensitivity analysis and process variations study.

TechModeler™, the first product of this flow, is a powerful tool that offers a definitive solution to behavioral modeling problems. Compared to classical and iterative methods (DoE, look-up tables, etc.), which are the most used in the industry, TechModeler™ offers accurate results for the most difficult problems. In order to reduce simulation cost, TechModeler™ gives an optimized coverage of the parameter space. Thus the tool incrementally generates a set of needed points for an efficient modeling. Models are automatically generated and validated as black-box models, but can also be developed through parts of semi-physical equation imposed by the physics.

TechSizer™, the second tool in the flow, is completely standalone software, easily integrable in every design environments. This tool allows the designers to automatically resize their circuits, thus drastically reducing costs and time-to-market.

TechAnalyzer™, the third product, is a powerful model-based analysis tool that provides the designer an easy and rapid sensitivity analysis of
the design. It provides different orders of sensitivity analysis, and let the designer compute Monte Carlo analysis with a consequent number of runs. Analysis over one million run is extremely common and done in seconds.

4. APPLICATION:

ST MICROELECTRONICS 65 NANOMETER LDO REGULATOR

4.1 Aim of the survey

When shrinking to 65 nanometer technology, the previously designed circuits and architectures must be resized to meet the new specifications.

The performances of the studied LDO regulator can be extracted with 2 different circuit benches and analysis: AC frequency analysis and transient analysis. This implies some methodological constraints to handle the results from the various netlists representing the benches of the circuit.

Some design variables as resistors and capacitors values have a predominant influence on some particular performances: gain margin, phase margin, Power Supply Rejection Ratio (PSRR) at different frequencies. The performances are also sensitive to temperature and voltage which have a wide range of variation. These environment parameters produce some non linear effects on the outputs which appear in a lot of cases.

In addition to these design and environment variables, the process parameters variations are also causing some spread on the performances.

Using the 65 nanometer design kit, there are 19 process parameters in the studied LDO regulator.

4.2 Modeling framework

4.2.1 Experimental protocol

The proposed flow was applied on a subset of all performances extraction with the following design and environment inputs:

- Design variables: the values of 2 resistors and 1 capacitor
- Environment variables: temperature (from -30 to 125 °C) and supply voltage (from nominal value 1.5 up to 1.7 V).

4.2.2 Modeling

40 samples data points were generated using TechModeler™ software for an optimal coverage of the parameters input space. For each sample, the spice simulation was launched and each performance extraction was computed. For the remainder of the study, 30 samples were sufficient to model accurately each performance. For some of them, less data points were sufficient. The last ones were kept for blind-validation of the models.

For each performance, the model can be displayed graphically in 2 dimensions.

Figure 1: behavioral schematic of the LDO regulator

To cover all the possible variations cases with a standard methodology, the simulation time is too long to achieve the study in a realistic time.

Using Lysis™ workflow, the aim of the survey is:
- To find a model for each circuit bench and analysis (AC frequency and transient analysis) based on design and environment variables variations.
- To optimize the input variables and find the best design point for these variables.
- To use the optimized values in the circuit and to find a model for process parameters, on which a sensitivity analysis and Monte Carlo simulation is launched with a high number of runs (> 1 million) within a realistic time.
set by the designer to consider that the generated model fits the spice simulation permits the acceptance of accurate models only.

The following errors between the model and the simulation were reported:

<table>
<thead>
<tr>
<th>Model</th>
<th>Mean relative error on modeling data</th>
<th>Mean relative error on validation data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase margin</td>
<td>0.34%</td>
<td>5.7%</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>0.41%</td>
<td>3.7%</td>
</tr>
<tr>
<td>PSRR 10Hz</td>
<td>0.1%</td>
<td>0.35%</td>
</tr>
<tr>
<td>PSRR 10KHz</td>
<td>0.28%</td>
<td>0.57%</td>
</tr>
</tbody>
</table>

Table 1: modeling results for Phase margin, gain margin and PSRR at 10Hz and 10 KHz

All the models will then be used for design variables sizing presented in the next section.

4.3 Sizing framework

TechSizer™ was used to optimize the design variables, so the performances specifications of the designer are met.

Some inputs and also performances constraints must be set according to the designer goal: nominal optimization, design centering…

<table>
<thead>
<tr>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
</tr>
<tr>
<td>VDD</td>
</tr>
<tr>
<td>MPhase</td>
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<tr>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Objectives</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSRR_10Hz</td>
</tr>
</tbody>
</table>

Table 2: Sizing objectives and constraints

Several constraints on the same performance have been defined (see Table 2) to find the best nominal optimization, like for example on the phase margin:
The voltage and temperature were set to the value considered as being the nominal point of the circuit. This specifications example shows some different types of requests TechSizer™ can support:

- Fixed value constraints: the VDD parameter has been constrained to 1.5V.
- Interval constraints: the R1 resistor value parameter has been constrained to a value between 13K and 21K.
- Multi-objective optimization: maximize the different PSRR and also the phase margin.

TechSizer™ sizing computation takes few minutes, and produces a report that gives the optimal point with a summary section containing the specifications attached with the given result. The design solution computed by TechSizer™ has been verified and validated with the STMicroelectronics golden spice simulator.

<table>
<thead>
<tr>
<th>Sizing results</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
</tr>
<tr>
<td>VDD</td>
</tr>
<tr>
<td>MPhase</td>
</tr>
<tr>
<td>PSRR 10Hz</td>
</tr>
<tr>
<td>PSRR 10KHz</td>
</tr>
</tbody>
</table>

**Table 3: Sizing results for some performances**

The design variables are fixed to these optimized values and are backannotated inside the TechModeler™ software to check the range of the performances with regard to voltage and temperature variations only. These parameters vary on their whole range to verify that the complete set of specifications is respected.

Now that the design variables are fixed, it is mandatory to check the validity and the sensitivity of the circuit to the process parameters.

### 4.4 Process parameters analysis

The same process flow explained above for design and environment variables was applied for process parameters involved in the design.

There are more process parameters than design and environment variables in the studied case: 19 process parameters are used in the library model card.

In the next step of the study, 90 samples were sufficient to model accurately the phase and gain margin. 10 extra points were kept for blind-validation of the models. For the different PSRR, 70 samples were enough to model them efficiently.

It should be noted that TechModeler™ generates a global model for the entire parameter space. This model, once obtained, can be used for many nominal and statistical computations. By contrast, projected posynomials modeling [10][11] is local and should be repeated for each computation.

Table 4 presents the number of samples needed by the different modeling methods.

<table>
<thead>
<tr>
<th>Modeling method</th>
<th>Parameters</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TechModeler</td>
<td>19</td>
<td>90</td>
</tr>
<tr>
<td>Posynomials [8][9]</td>
<td>19</td>
<td>625</td>
</tr>
<tr>
<td>Projected posynomials [10][11]</td>
<td>19</td>
<td>154</td>
</tr>
</tbody>
</table>

**Table 4: Number of samples needed for modeling**

As TechModeler™ allows an incremental generation of optimal parameters samples, we first generated 50 samples to check out the design. As no acceptable model could be computed with these samples (mean relative error on modeling and validation data were out of acceptable range), a new set of 20 samples was generated. This was done twice until the acceptation criteria were reached.

Thanks to the TechModeler™ display viewer, some non-useful parameters were detected early in the process evaluation phase and could be ignored during the modeling step.

The generated models were used to find exactly which process parameters the circuit is sensitive to.
This allows checking the yield of the circuit for each performance in a realistic time.

All these features will help the designer to validate the robustness of his design.

4.5 Sensitivity analysis framework

With the generated model, TechAnalyzer™ offers the possibility to speed up the Monte Carlo analysis and also to evaluate the sensitivity of the design to process parameters. The software is using the models generated previously with TechModeler™ and also the distribution type and range of each process parameter. All distribution types are supported: uniform, gaussian and lognormal.

Based on the model, several Monte Carlo analyses were done thanks to the very fast computation time it required.

5000 Monte Carlo runs were done to compare versus real spice Monte Carlo. Please note that we had to limit this comparison to a 5000 Monte Carlo run due to the length of the real spice Monte Carlo.

Figure 4: Monte Carlo Gain Margin with spice Monte Carlo and Infiniscale fast Monte Carlo

The mean and sigma values as well as the min and max spread are comparable. More than 8 hours spent with the spice Monte Carlo methodology was decreased to a few seconds with model-based Monte Carlo.

Moreover, to evaluate the yield of the performances and also to all entries combinations, some other fast Monte Carlo were launched. Using TechAnalyzer™, the designer evaluated the occurrence of some extreme cases that were missed with the limited Monte Carlo. It appeared that min and max values can change between 5000 and 1 million Monte Carlo runs. The 1 million Monte Carlo run took less than a minute to compute with TechAnalyzer™. The number of occurrences that are out of specifications can therefore be quantified and corrected if relevant.

To assist the designer when reducing the spread of the performances dispersions due to the process parameters, a sensitivity analysis is performed. This step is done in TechAnalyzer™ too. It provides the relative weight of each process parameter in the performances dispersions. This information is very useful to analyze the dominant process parameters and so, give the designer a chance to reduce the influence of the parameter. Thanks to this step, a correlation between process and design can be done to improve spread dispersion of the performance.

<table>
<thead>
<tr>
<th></th>
<th>Gain margin sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nmos vt and mobility</td>
<td>43%</td>
</tr>
<tr>
<td>Poly variation</td>
<td>43%</td>
</tr>
<tr>
<td>Poly resistor w and l variations</td>
<td>12%</td>
</tr>
</tbody>
</table>

Table 4: Sensitivity analysis for Gain Margin

At the beginning of the study, 19 process parameters were used in the model cards for this LDO regulator design. The study shows that only 3 have an impact on the gain margin performance. This information can also be used to check if some parameters are dominant on other performances and adjust all of them, taking into account all the shared effects.

5. CONCLUSION

In this article, the InfiniScale flow for a complete solution of modeling, sizing and analysis of analog designs is described, and successfully applied to a STMicroelectronics LDO regulator design. Accurate models for design and environment variables were obtained using TechModeler™ software, and a robust design has been sized taking into account all these parameters, using TechSizer™. Once the nominal design was found, some other accurate
models have been generated to manage the process parameters variations accurately and quickly. The design sensitivity to process parameters has been analyzed and a huge number of Monte Carlo runs were computed in a very short time with TechAnalyzer™ software.

The complete InfiniScale flow allows the designer to efficiently model his designs, and size them optimally according to the specifications. Then the influence of process parameters can be analyzed precisely and rapidly, allowing yield problems detection during the design phase, for upfront detection instead of late catch-up.

This innovative methodology and workflow improved both the quality of the design and the productivity of the designer.

6. REFERENCES

[1] InfiniScale: http://www.infiniscale.com